

CLAIMS

1. A semiconductor device comprising:

a first interlayer insulating film formed on a semiconductor substrate, the surface of said first interlayer insulating film being leveled;

a plurality of conductor plugs which are formed by filling each of a plurality of openings formed in said first interlayer insulating film so as to be level with said surface of said first interlayer insulating film;

a second interlayer insulating film formed on said surface of said first interlayer insulating film and of said conductor plugs;

a wiring pattern formed on said second interlayer insulating film;

a third interlayer insulating film formed on said second interlayer insulating film so as to cover said wiring pattern; and

a plurality of interconnect conductors formed by filling each of a plurality of the openings penetrating said second and third interlayer insulating films to said conductor plug, said interconnect conductors being electrically connected to each of said conductor plugs.

2. The semiconductor device as defined in claim 1, wherein said interconnect conductor is formed so as to have an enlarged diameter over said third insulating film, said interconnect conductor working as an electrode for storing electrical charge.

3. The semiconductor device as defined in claim 1, wherein said first interlayer insulating film is comprised of a silicon oxide film containing at least phosphor.

4. The semiconductor device as defined in claim 1, wherein the conductor film is comprised of polycrystalline silicon or amorphous silicon.

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5. A semiconductor device comprising:

a first interlayer insulating film continually formed on first and second regions of a semiconductor substrate, the surface of said first interlayer insulating film being leveled at least in said first region;

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a plurality of conductor plugs formed at least in said first region by filling openings formed in said first interlayer insulating film so as to be flush with said surface of said first interlayer insulating film;

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a second interlayer insulating film continually formed on said first interlayer insulating film and said conductor plugs so as to extend over said first and second regions;

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a wiring pattern formed on said surface of said second interlayer insulating film in at least said first region;

a third interlayer insulating film formed on said surface of said second interlayer insulating film so as to cover said wiring pattern; and

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a plurality of interconnect conductors formed in at least said first region by filling each of said openings penetrating said second and third interlayer insulating films to each of said conductor plugs, said interconnect conductors being electrically connected to each of said conductor plugs.

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6. The semiconductor device as defined in claim 5, wherein said first region is formed as a memory array

region; said second region is formed as a logic circuit region; and said interconnect conductor is formed to have an enlarged diameter over said third interlayer insulating film as an electrode for storing electrical charge.

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7. The semiconductor device as defined in claim 5, wherein said first interlayer insulating film is comprised of a silicon oxide film containing at least phosphor.

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8. The semiconductor device as defined in claim 5, wherein said conductor film is comprised of polycrystalline silicon or amorphous silicon.

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9. A method of manufacturing a semiconductor device comprising the steps of:

forming a first interlayer insulating film on a semiconductor substrate;

forming a plurality of openings in said first interlayer insulating film;

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forming a conductor film on said first interlayer insulating film so as to fill said openings;

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removing said conductor film from said surface of said first interlayer insulating film through chemical etching and forming conductor plugs from said conductor film filled in said openings; and

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leveling the surface of said first interlayer insulating film from which said conductor film has been removed until the surface of said first interlayer insulating film becomes flush with the surface of said conductor plugs by chemical-and-mechanical polishing.

10. The semiconductor device manufacturing method

as defined in claim 9, further comprising the steps of:

forming a second interlayer insulating film on said first interlayer insulating film having said conductor plugs formed therein;

5 forming a wiring pattern on said second interlayer insulating film;

forming a third interlayer insulating film on said second interlayer insulating film so as to cover said wiring pattern; and

10 forming a plurality of openings so as to penetrate said second and third interlayer insulating films respectively to said conductor plugs; and

forming a plurality of interconnect conductors in said openings so as to be electrically connected to each of said conductor plugs.

11. The semiconductor device manufacturing method as defined in claim 9, wherein said first interlayer insulating film is formed from a silicon oxide film containing at least phosphor.

12. The semiconductor device manufacturing method as defined in claim 9, wherein said conductor film is formed of polycrystalline or amorphous silicon.

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13. A semiconductor device manufactured by the semiconductor device manufacturing method as defined in claim 9.